REMARKS

This reply is filed in response to the Office Action dated October 5, 2006, citing formal objections to claims 1 – 51 and 57 – 63, and rejecting claims 1 – 63 under 35 U.S.C. § 112 and 35 U.S.C. § 103. In view of the amendments above and the remarks that follow, the Applicants submit that all pending claims are in condition for allowance.

I. All Grounds for Objection to the Claims are Removed

The claims are amended to address the Examiner's objections. Independent claims 1, 7, 17, 28, 32, 35, 41, 47, 57 and 61 are amended to recite, amongst other things, that one or more processes or threads are collectively referred to as "threads." Claims 7, 17 and 41 are amended to include periods at the end of the claims. Claim 17 is further amended to recite, "each thread being any of constrained or not constrained to execute on a same virtual processing unit" in ¶ B, and replace "processing units" with "virtual processing units" in ¶ C. Claim 41 is also amended to recite proper antecedent basis for "execution units." Claims 36, 48 and 62 are amended to recite, "processing the event by the thread to which the event is delivered," as suggested by the Examiner.

In view of the above, the Applicants request that all formal objections be withdrawn.

II. The Claims are in Full Compliance with 35 U.S.C. § 112

Claims 17 – 27, 36, 48 and 62 stand rejected under 35 U.S.C. § 112, second paragraph. The claims are amended to comport with Examiner's suggested amendments and 35 U.S.C. § 112. Claim 17 is amended to recite, among other things, "each thread being any of constrained

or not constrained," and replace "the plurality of processing units" with "the plurality of virtual processing units." Claims 36, 48 and 62 are amended to recite, "processing the event by the thread to which the event is delivered."

In view of these amendments, the Applicants request that all 35 U.S.C. § 112 rejections be withdrawn.

III. Rejection of Claims 1 – 3, 5 – 14, 16 – 23, 27 – 37, 39 – 52 and 56 – 63 Under 35 U.S.C. § 103

The captioned claims stand rejected as allegedly unpatentable over Brown, III et al. (US 6,240,508 B1; hereinafter "Brown") in view of Jagannathan et al. (US 5,692,193; hereinafter "Jagannathan").

Independent Claim 1

Claim 1 is directed towards an embedded processor comprising a plurality of processing units that each execute processes or threads (collectively, "threads"). One or more execution units are shared by the processing units and execute instructions from the threads. An event delivery mechanism that is in communications coupling with the plurality of processing units and delivers events (e.g., interrupts) to respective threads without execution of instructions by the processing units.

Neither Brown nor Jagannathan, either individually or in combination, disclose an embedded processor meeting the limitations of claim 1. Moreover, the record is devoid of evidence suggesting any motivation to combine the references.

Brown purports to improve processor performance by teaching a synchronized macropipelined microprocessor chip, and purports to disclose a CPU having several distinct "units," including an "execution unit." *See,* Brown, col 7, lines 24 – 48. Nowhere does it teach or suggest an event delivery mechanism that is in communication with a plurality of processing units and that delivers events to respective threads without execution of instructions by the processing units, The Examiner does not contend otherwise.

Jagannathan fails to remedy the deficiencies of Brown. Jagannathan is directed to a software architecture for the control of highly parallel computer systems. Although it purports to disclose an event delivery mechanism, nowhere does that publication teach or suggest such a mechanism that meets the limitations of the claimed invention — e.g., one that can deliver events without execution of instructions by processing units.

In contrast, Jagannathan only purports to disclose an "exception dispatcher" within the operating system ("Sting"). This uses an exception "handler to decide which thread to run next on the processor." *See* Jagannathan, col. 24, line 62, to col 25, line 29. Handlers, according to that publication, "are procedures that execute within a thread." *See* Jagannathan, col. 24, lines 12 – 13. Hence, they necessarily require instruction execution. The claimed invention explicitly eschews this.

Moreover, there is no motivation to combine Brown and Jagannathan. Brown is purportedly directed towards processor improvements in the physical hardware of a microprocessor. The delivery mechanism of that publication is accordingly implemented at the hardware level. *See,* Brown, col 14, lines 1 – 17 and col 7, lines 24 – 48. Jagannathan, on the

other hand, is directed towards features which are several abstraction layers above the hardware level: the delivery mechanism, which is implemented at the operating system level, is one example of this.

It would not have been obvious to one of ordinary skill in the art to combine features of a delivery mechanism implemented at the hardware layer with a delivery mechanism implemented at the operating system layer. Nor is there be motivation to do so.

Further, even if such motivation existed, the cited references lack sufficient teachings to make the combination possible or fathomable. Thus, there is nothing in the record that suggests how features of Jagannathan's operating system implementation might be co-implemented with Brown's hardware delivery mechanism.

In view of the foregoing, it is evident that the combination of Brown and Jagannathan fails to teach, suggest or otherwise render unpatentable the subject matter of claim 1. The same is true for claims 2, 3, 5 and 6 which depend from claim 1 and recite further limitations thereon.

Independent Claims 17, 28, 32, 35, 41, 47, 57, 61

The above independent claims recite *inter alia* an event delivery mechanism that is in communication coupling with a plurality of processing units (or "virtual processing units" in claims 17, 32, 41, 47 and 61) and that delivers events to respective threads with which those events are associated without execution of instructions by said processing units (or "virtual processing units" in claims 17, 32, 41, 47 and 61). For at least the reasons discussed above, Brown and Jagannathan, individually or in combination, fail to teach or suggest an event delivery mechanism with such limitations.

In view of the foregoing, it is evident that the combination of Brown and Jagannathan fails to teach, suggest or otherwise render unpatentable the subject matter of independent claims 7, 17, 28, 32, 35, 41, 47, 57, 61.

The same is true for claims 8 – 14, which depend from claim 7 and recite further limitations thereon; claims 18 – 23, which depend from claim 17 and recite further limitations thereon; claims 29 – 31, which depend from claim 28 and recite further limitations thereon; claims 33 and 34, which depend from claim 32 and recite further limitations thereon; claims 36, 37, 39 and 40, which depend from claim 35 and recite further limitations thereon; claims 42 – 46, which depend from claim 41 and recite further limitations thereon; claims 48 – 56, which depend from claim 47 and recite further limitations thereon; claims 58 – 60, which depend from claim 57 and recite further limitations thereon; and claims 62 and 63, which depend from claim 61 and recite further limitations thereon.

IV. Rejection of Claims 4, 24 – 26, 38 and 53 – 55 Under 35 U.S.C. § 103

Dependent claims 4, 24 – 26, 38 and 53 – 55 stand rejected as allegedly unpatentable over Brown in view of Jagannathan, and further in view of Eggers (Eggers et al. "Simultaneous Multithreading: A Platform for Next-Generation Processors," IEEE, 1997; pages 12 – 29).

As discussed above, Brown and Jagannathan, both individually or in combination, fail to teach or suggest *inter alia* the event delivery mechanism of the claimed invention, as described above. Eggers does not teach or suggest a delivery mechanism with such limitations. The Examiner does not assert otherwise.

Accordingly, dependent claims 4, 24 – 26, 38 and 53 – 55 stand free and clear of the

combined teachings of Brown, Jagannathan and Eggers. The 35 U.S.C. § 103 rejection should, therefore, be withdrawn.

V. Rejection of Claim 15 Under 35 U.S.C. § 103

Dependent claim 15 stands rejected as allegedly unpatentable over Brown in view of Jagannathan, and further in view of Gosior et al. (US 2003/0120896 A1; hereinafter "Gosior").

As discussed above, Brown and Jagannathan, both individually or in combination, fail to teach or suggest *inter alia* the event delivery mechanism of claim 7, as described above. Gosior does not teach or suggest such a mechanism – nor does the Examiner contend otherwise.

Accordingly, claim 15 stands free and clear of the combined teachings of Brown, Jagannathan and Gosior. The 35 U.S.C. § 103 rejection should, therefore, be withdrawn.

VI. Conclusion

In light of the foregoing, Applicants believe that the application is in condition for allowance. The Examiner is encouraged to telephone the undersigned attorney for Applicants if such communication will expedite prosecution of this application.

Respectfully submitted,

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